What is claimed is :

1. A circuit for processing charge detecting signal transferred to a floating diffusion amplifier from a charge coupled device, said circuit comprising :

a first node connected to said floating diffusion amplifier ;

a first enhancement type field effect transistor being connected in series between a first fixed-voltage supply line for supplying a first fixed voltage and an output terminal, and said first enhancement type field effect transistor having a first gate connected to said first node ; and

a second enhancement type field effect transistor being connected in series between a second fixed-voltage supply line for supplying a second fixed voltage and the output terminal,

wherein said second enhancement type field effect transistor has a second gate supplied with a third fixed voltage which is different in potential from said second fixed voltage.

2. The circuit as claimed in claim 1, wherein said second gate of said second enhancement type field effect transistor is connected to said first fixed-voltage supply line, and said second gate is supplied with said third fixed voltage which is equal to said first fixed-voltage.

3. The circuit as claimed in claim 2, wherein said first fixed-voltage supply line comprises a power voltage line, whilst said

second fixed-voltage supply line comprises a ground line.

4. A circuit for processing charge detecting signal transferred to a floating diffusion amplifier from a charge coupled device in response to a transfer gate clock signal, said circuit comprising :

a first node connected to said floating diffusion amplifier ;

a first enhancement type field effect transistor being connected in series between a first fixed-voltage supply line for supplying a first fixed voltage and an output terminal, and said first enhancement type field effect transistor having a first gate connected to said first node ;

a second enhancement type field effect transistor being connected in series between a second fixed-voltage supply line for supplying a second fixed voltage and the output terminal, and said second enhancement type field effect transistor having a second gate connected to a second node ; and

a voltage control circuit being connected to said second node for connecting said second node to a third fixed-voltage in a first time period, in which said transfer clock signal is not supplied, and also for electrically isolating said second node from said third fixed-voltage in a second time period, in which said transfer clock signal is supplied.

5. The circuit as claimed in claim 4, wherein said voltage control circuit includes a capacitance connected in series between said second node and said second fixed-voltage supply line for fixing said second node in

potential.

6. The circuit as claimed in claim 4, wherein said voltage control circuit further includes :

a voltage dividing circuit being connected in series between said first fixed-voltage supply line and said second fixed-voltage supply line ;

a third node connected to an output terminal of said voltage dividing circuit ; and

a third enhancement type field effect transistor being connected in series between said second and third nodes, and said third enhancement type field effect transistor having a gate receiving a control signal under which said voltage control circuit is operated.

7. The circuit as claimed in claim 6, wherein said control signal comprises said transfer gate clock signal.